



PTO/SB/08A (08-03)

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 3

Complete if Known

Application Number	10/521,889
Filing Date	May 25, 2005
First Named Inventor	William ROBBINS
Art Unit	2133
Examiner Name	Unassigned
Attorney Docket Number	0903-003

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US 5,253,308	10/12/1993	JOHNSON	
		US 4,601,031	07/15/1986	WALKER et al.	
		US 4,603,404	07/29/1986	YAMAUCHI et al.	
		US 5,795,797	08/18/1998	CHESTER et al.	RECEIVED JUN 29 2005
		US 4,858,233	08/15/1989	DYSON et al.	
		US 2002/0174318 A1	11/21/2002	STUTTARD et al.	Technology Center 2100
		US 5,796,937	08/18/1998	KIZUKA	
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FOREIGN PATENT DOCUMENTS

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		WO 01/02960 A1	01/11/2001	CLERMIDY et al.		
		WO 02/50624 A2	06/27/2002	CLAYDON et al.		
		WO 91/11770	08/08/1991	LEGENDI et al.		
		EP 0 180 212 A2	05/07/1986	EATON et al.		

Examiner Signature	/Michael Maskulinski/	Date Considered	06/05/2008
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NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	1	Popli, S. P., et al., "A Reconfigurable VLSI Array for Reliability and Yield Enhancement," Proceedings of the International Conference on Systolic Arrays, 1988, pp. 631-642.	
	2	John, L. K., et al., "A Dynamically Reconfigurable Interconnect for Array Processors," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 6, No. 1, March 1998, pp. 150-157.	
	3	Shigei, N., et al., "On Efficient Spare Arrangements and an Algorithm with Relocating Spares for Reconfiguring Processor Arrays," IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, Vol. E80-A, No. 6, June 1997, pp. 988-995.	
	4	Schmidt, U., et al., "Datawave: A Single-Chip Multiprocessor for Video Applications," IEEE Micro, Vol. 11, No. 3, June 1991, pp. 22-25, 88-94.	
	5	Chean, M., et al., "A Taxonomy of Reconfiguration Techniques for Fault-Tolerant Processor Arrays," Computer, IEEE Computer Society, Vol. 23, No. 1, January 1990, pp. 55-69.	
	6	Kamiura, N., et al., "A Repairable and Diagnosable Cellular Array on Multiple-Valued Logic," Proceedings of the 23rd International Symposium on Multiple-Valued Logic, 1993, pp. 92-97.	
	7	LaForge, L., "Extremely Fault Tolerant Arrays," Proceedings: International Conference on Wafer Scale Integration, 1989, pp. 365-378.	

Examiner Signature	/Michael Maskulinski/	Date Considered	06/05/2008
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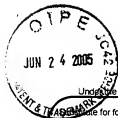
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STATEMENT BY APPLICANT**

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Sheet 3 of 3

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	8	International Search Report of PCT/GB03/02772, dated November 30, 2004.	
	9	Great Britain Search Report of Application No. GB 0216880.5, dated January 28, 2003.	
	10	Great Britain Search Report of Application No. GB 0216880.5, dated October 9, 2003.	
	11	Great Britain Search Report of Application No. GB 0216880.5, dated April 1, 2005.	

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